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COMPARISON OF SYNCHRONIZATION TECHNIQUES FOR THE AFIT DIRECT SEQUENCE SPREAD SPECTRUM SYSTEM

THESIS

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THESIS

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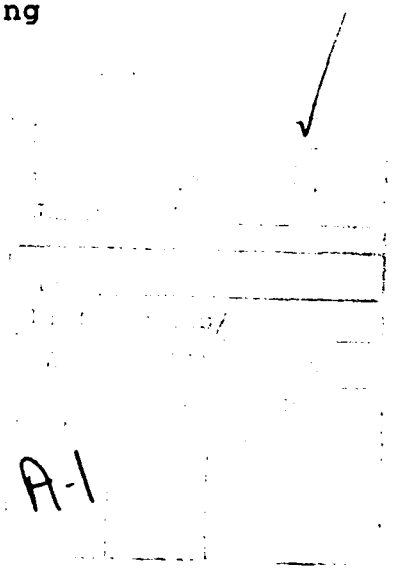

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Table of Contents

List of Figures

Abstract

The purpose of this study is to analyze and evaluate the performance of several code synchronization methods that could be used in the Air Force Institute of Technology's (AFIT) Direct-Sequence Spread Spectrum (DSSS) communication system. These methods include the sliding correlator, transmitted reference, sequential estimation, and three types of matched filters. The matched filters are the baseband matched filter, delay line matched filter, and the convolver.

The criteria used for the evaluation of these synchronization methods are theoretical synchronization times and probability of bit-error. Advantages and disadvantages of each synchronization method are described and a method is recommended to be tested in the existing AFIT DSSS system prototype.

The effect of adding a PLL circuit to the AFIT system needs to be investigated, especially the effect on the bit-error curve measured by James Stephens when he built the AFIT system. A matched filter convolver should be added in place of the synchronous oscillator and its effects analyzed.

Comparison of Synchronization Techniques for the AFIT Direct Sequence Spread Spectrum System

I. Introduction

Background

Spread Spectrum Modulation is rapidly growing in interest to the Department of Defense (DoD) as a form of communication system. The major reasons for this interest are that a spread spectrum modulation system provides the advantages of anti-jam (AJ) capability and low probability of intercept (LPI) (13:538-542). A spread spectrum system uses a large bandwidth to transmit information with a narrow bandwidth. A code, independent of the information being transmitted, is used to achieve this large bandwidth. While it is true that bandwidth is a finite resource and must be conserved, it is this large bandwidth that gives the AJ and LPI advantages found in spread spectrum modulation (1:17).

The DoD has been investigating military uses for spread spectrum systems for years. Most of the details of these applications are classified. Space and other civilian applications are usually proprietary and few articles

dealing with practical details of spread spectrum systems have been published. The majority of articles deal with block diagrams of systems and mathematical equations (7:14).

In a previous thesis, a Direct Sequence Spread Spectrum (DSSS) system was built by James Stephens to demonstrate and evaluate DSSS system parameters and performance (14). Because of its modular design, this system can be used as a test-bed for evaluating DSSS system subcomponents. It will be referred to as the AFIT system in this thesis.

The direct sequence technique uses a pseudo-noise (PN) digital code to directly modulate a conventional frequency modulated (FM) carrier in the AFIT system. PN codes exhibit random properties which are used to provide the signal security and good spectral characteristics required of the communication system. These code sequences can be as short as a few hundred bits or longer than 2^{89} bits. The rate at which the code is generated can stretch from a dozen bits per second to several gigabits per second. The output of the PN code generator is a sequence of chips. The processing gain in a direct sequence system is proportional to the number of chips per data bit. This is the ratio of the spread bandwidth to the data bandwidth (13:555). In low cost systems, such as the AFIT system (14), this ranges from

15 to 63 chips per bit. This represents a theoretical maximum processing gain of 11.8 dB to 18 dB (11:97). The longer the pseudo-random code is, the lower the power spectral density and the more difficult the signal is to intercept and decode.

Problem

The major problem in the DSSS system is that of synchronizing the PN code of the receiver with that of the transmitter. In a DSSS system, code synchronization is the aligning of the transmitter code reference and the receiver code reference, chip for chip. Once code synchronization occurs, the information (data) can be demodulated from the received signal (4:217).

Code synchronization is required in direct-sequence spread spectrum systems because the PN code is the key to despreading the received signal, spreading any undesired signals, and recovering the information that was transmitted (1:214). PN code synchronization must be performed prior to carrier synchronization, because the signal-to-noise ratio of the spread signal is typically too low to allow carrier synchronization (15:524). Synchronization errors, such as

false synchronization lock and PN code clock jitter, degrade the performance of the system. In digital systems, the bit error rate is the measure of performance of the system and is strongly affected by imperfect code synchronization.

Research Objectives

The objective of this thesis is to analyze and predict the performance of several different synchronization techniques, including the phase-locked loop (PLL), in a direct-sequence spread spectrum system. A recommendation will be made as to which synchronization technique shows the most promise of improving the AFIT system. The AFIT DSSS system is constructed in a modular form, which facilitates the installation and checkout of proposed synchronization methods, possibly as a follow on to this thesis.

The range of the AFIT DSSS system is approximately 100 feet. While the synchronous oscillator in the AFIT system does synchronize and track the incoming signal satisfactorily, there is room for improvement. A more conventional synchronization method may provide a greater range for the system. This system also provides an educational benefit to the students at AFIT.

Research Questions

Several research questions are answered in this thesis. Among them are the theoretical synchronization time and bit-error rate of several alternate synchronization methods in the AFIT DSSS system. The phase-locked loop is another synchronization technique, and its effect on synchronization time is analyzed. The bit-error rate and synchronization time of the synchronous oscillator is compared to several other synchronization techniques. The advantages and disadvantages of each are discussed and a recommendation made on which one should be tested on this system.

Summary of Current Knowledge

The AFIT DSSS system transmits on amateur radio frequencies and therefore must comply with certain legal restrictions.

The Law. In 1985 the Federal Communications Commission wrote a new regulation, 15.126, governing the spread spectrum system form of communications product. This regulation allowed the unlicensed operation of a spread spectrum communications system, direct sequence or frequency

hopping, with a maximum power of 1 watt, for certain specified frequency ranges (11:96).

Trade-offs. As with any type of communication system, there are advantages and disadvantages to the spread spectrum system. Some of the advantages not available in any other form of communication system include: selective addressing capability; code division multiplexing; low power spectral density output signals; inherent message security; and interference rejection. It is the message security and low probability of intercept aspects of the advantages that appeal to the military services (2:1-3).

On the negative side, a spread spectrum system employs much more bandwidth than a narrowband communication system using AM or FM. The system is also more complex in that it requires code sequence generators, tracking loops, matched filters, and other subsystems not usually found in a more conventional system (2:1).

Spectral Characteristics. A DSSS system signal can be obtained by combining an FM signal with the output of a pseudo-noise (PN) code generator. A doubly balanced mixer (DBM) performs this task. The DBM performs the function of multiplying the PN code and the FM signal. Its output is a

Binary Phase-Shift-Keyed (BPSK) signal (14:27). This BPSK signal is centered at the carrier frequency, with a $[(\sin x)/x]^2$ frequency spectrum. The original carrier is suppressed. The main lobe of this spectrum has a null-to-null bandwidth that is twice the clock rate of the PN code, while the null-to-null bandwidth of the sidelobes equals the PN clock rate. At the receiver, another DBM combines the incoming signal with the known PN code. This results in the received signal being "despread" and the transmitted signal being recovered (2:1). This also has the added benefit of spreading out any undesirable signals that may be received with the transmitted signal.

Synchronizers. According to Dixon, "More time, effort, and money has been spent developing and improving synchronizing techniques than in any other area of spread spectrum systems" (1:214). Different types of code synchronization studied in this thesis include: convolvers; sliding correlators; matched filters; sequential estimation; and transmitted references.

Present Uses. A digital matched filter is being used in the Joint Tactical Information Distribution System for code synchronization. Some types of convolvers are capable of wide bandwidths and are inexpensive, which makes them

attractive for commercial applications. The DoD's Very High Speed Integrated Circuit (VHSIC) program is aiding digital matched filter technology. Hughes Aerospace and TRW are developing VHSIC digital matched filters (12:20). It is expected that digital matched filters will dominate the below 25 MHz PN spreading rate market in the latter part of this decade, while the convolvers will dominate the above 60 MHz market. Other forms of the matched filter will be used at spread rates between the low and high ends of the market (12:19-20).

Comparison of IEEE Synchronous Oscillator Letters.

The AFIT system uses a synchronous oscillator for the acquisition and tracking of the incoming signal. This type oscillator was pioneered by Uzunoglu and White. A letter by these two authors appeared in the March 1986 Proceedings of the IEEE, with a counter letter by Gardner. Gardners' letter refutes the claims of Uzunoglu's and Whites' letter on the advantages of synchronous oscillators (4:1121-1122) (16:516-517). Uzunoglu claims, and proves with equations and deductions from experiments, that the synchronous oscillator (SO) is a device able to lock onto a sinusoidal signal quickly but still apply the long-term averaging needed to reject noise. The SO is described as an adaptive filter with low resolution bandwidth. It has the ability to

lock onto the injected carrier, within the tracking range, with high noise rejection while maintaining a wide tracking range. Gardner points out several discrepancies in the Uzunoglu letter, starting with the basic equation for the phase of the SO (4:1121). The claim by Gardner is that this equation is identical to the differential equation of a first order phase-locked loop, and the SO performance should be the same as a PLL. While true that in certain areas of operation the SO follows the operation of an injection oscillator, basically a PLL, the equation for the SO was derived from an SO equivalent circuit. This circuit is nonlinear, and the linearization of a nonlinear system results in qualitative results (4:1123).

Several discrepancies were explained as improper preparation of the letter prior to publication. Incorrect photographs and figures were accidentally placed in the Uzunoglo and White letter.

The synchronization time equation, used in the theoretical calculation of the SO in Chapter IV, was obtained from the letter Gardner disputes. He claims that much longer synchronization times are likely because the initial phase of the system must be taken into account. The acquisition time in an SO depends on the initial frequency

difference and the tracking range, not on the resolution bandwidth (4:1123). Uzunoglus' experiments indicate that the acquisition time is much faster than a first order PLL, due to the high regeneration gain and direct feed of the synchronization signal.

Criteria

The criteria used to determine synchronization performance are synchronization time and bit-error rate. The standards for determining synchronization performance are the same as those in (14). These are the success of achieving synchronization and the time required for obtaining initial synchronization (14:18). In this way, a more accurate comparison is made with Stephens' work to give the reader a better insight into the theoretical performance of the methods examined here.

Scope

This work is limited to the synchronization section of the AFIT system only. An overall AFIT DSSS system description is not included in this work as that is readily available in Stephens' work (14).

Report Organization

Chapter II is a background review containing a definition of synchronization, a description of the synchronization methods examined, and a description of the phase-locked loop methods that were evaluated. Chapter III discusses PLL implementation and several circuits that would work in the AFIT system. A recommendation of the PLL IC that should be implemented is given here. Chapter IV contains the theory of operation, including mathematical formulas, for the performance of alternate synchronization methods. It also includes theoretical synchronization times and parameters of the synchronous oscillator used by Stephens. Chapter V contains comparisons between the synchronization methods and Stephens results. Chapter VI presents specific information needed to develop an implementation method for the PLL in the AFIT system. Chapter VII includes conclusions and additional comments.

II. Background

This chapter gives a definition of synchronization and describes in detail the different synchronization techniques considered for implementation in the AFIT system. The phase-locked loop is a synchronization tool and its description is included.

Definition

Synchronization is the aligning of a receiver's locally generated waveform with the spreading modulation superimposed, by the transmitter, on the incoming signal. This results in despreading of the incoming signal. The synchronization process is often considered to be composed of two parts: acquisition and tracking (12:7).

Acquisition involves a search of the region of time-frequency uncertainty and a determination that the locally generated code and incoming code are aligned closely enough (12:7).

Tracking is the process of maintaining the alignment of the two signals. This typically is accomplished by using some form of feedback loop which also reduces the alignment error present after acquisition (12:7).

Sliding Correlator

The sliding correlator is algorithmically the simplest synchronization technique in use (1:218). Its name is derived from the fact the receiver operates its code sequence generator at a slightly different rate from that of the transmitter. The result is the two code sequences "slide," in time, past each other, and are made to stop only when they match up. Upon match up, a code sequence output signal is generated which is of sufficient amplitude to lock the clock at its then present frequency, and enable the tracking feedback loop. The demodulator must then acquire carrier lock on the incoming signal. Figure 1 shows a flow diagram for a sliding correlator synchronizer (1:218-221).

An advantage of this synchronization technique is its simplicity. Nothing more than some controlled way of shifting the rate of the receiver code clock is needed.

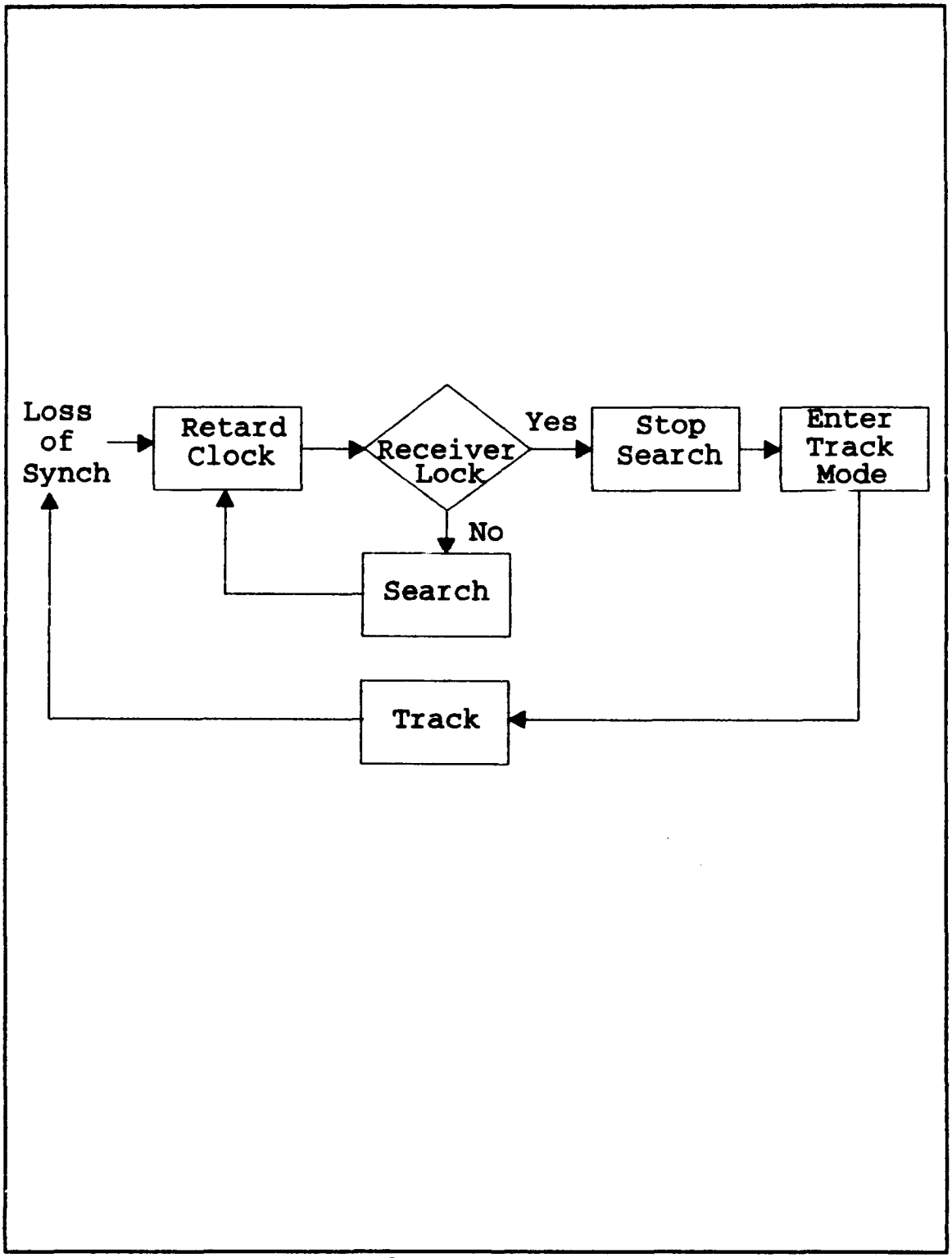

Figure 1. Flow Diagram for a Sliding Correlator Receiver.

The disadvantage of the sliding correlator becomes evident when a large degree of uncertainty is encountered. It is not practical to check the total number of code-phase positions because of the length of time required to accomplish this.

The search rate of a sliding correlator is limited by the baseband receiver bandwidth. Recognition of synchronization, which must occur to stop the sliding process at or near synchronization, is limited in its response time. If the search rate is too fast, the signals will slide through the point of correlation before the "lock" signal enables the tracking loop and stops the code generator clock at its then present frequency. For example, if the postcorrelation receiver bandwidth was 1 KHz, and using the rise time-to-bandwidth relationship of $T_R=0.35/BW$, the system could theoretically achieve synchronization in 350 μs. The time used to slide through the point of correlation should be a minimum of this amount. The correlation function is two chip durations wide. Also, the maximum search rate, $2/T_R$, would be approximately 5.7 Kbps. Generally, the search rate is equal to the data rate for which the receiver was designed (1:221).

Transmitted Reference

Some of the least complex receiver systems in use today employ the transmitted reference method of synchronization. This method could be used for acquisition and/or tracking. The receiver has no stored pseudo-noise code or code generator. The coded reference is generated and sent, along with the data message, at the transmitter. The coded reference and the data message are at two different frequencies. Figure 2 shows a block diagram of the transmitted reference synchronization technique. FC_1 and FC_2 are the two carrier frequencies separated by the intermediate frequency (IF) frequency. RF_1 and RF_2 are recovered carriers also separated by the IF frequency.

The receiver operation is identical to any other receiver using an offset local reference signal. The difference is that the local reference is generated at the transmitter and transmitted along with the signal to be demodulated. The frequencies of their carriers are offset by an amount that equals the first IF of the receiver. When these signals are mixed an IF signal is produced. Since the time delay of both the transmitted spread signal and the reference are the same, the mixer despreads and is correlated.

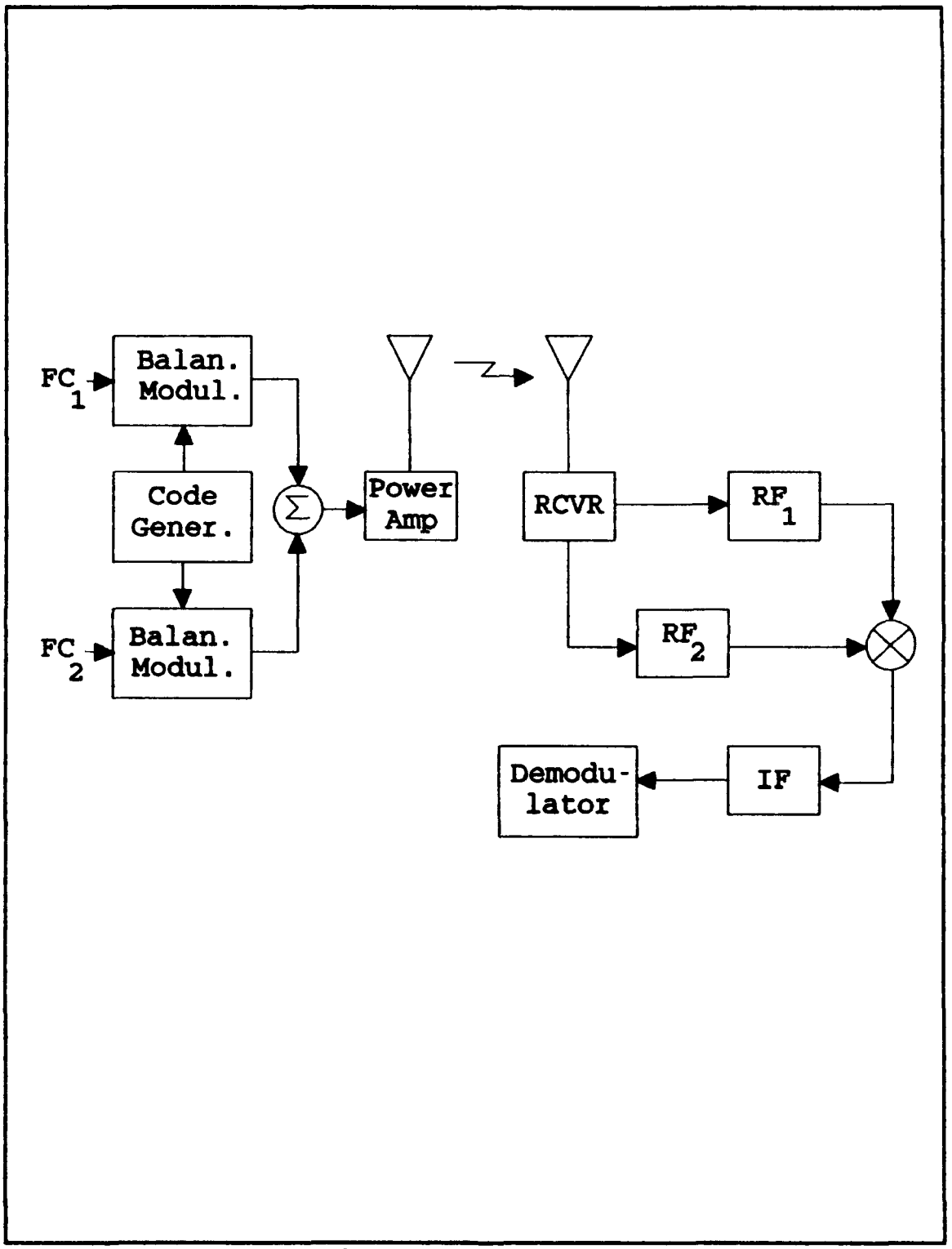

Figure 2. Transmitted Reference Synchronization Diagram.

The greatest advantage of the transmitted reference method is the ability to build a receiver that is smaller, lighter, and cheaper. This is possible due to the lack of code sequence generators, tracking circuits, and related circuits.

The biggest disadvantage is the ability to interfere and/or jam the message signal. Any two identical signals separated by the receiver's first stage IF frequency would produce a false synchronization. It is possible to protect against this by frequency hopping one of the transmitted signals, but this would defeat the main advantage by adding cost, complexity, and increasing the time it takes for synchronization to occur. Another disadvantage is the noise that is introduced onto the transmitted reference from the transmitter and transmission medium. This noise will degrade signal demodulation, sometimes drastically (1:224).

Sequential Estimation

In sequential estimation, the receiver demodulates the incoming coded signal. The signal is demodulated in the same way as any phase shift keyed (PSK) data stream is demodulated. The demodulated chips are used as an initial

fill of the PN generator. and a check made for successful synchronization. If synchronization did not occur, another set of demodulated chips is loaded into the PN generator and synchronization checked. The process is repeated until synchronization occurs. It may not be a simple task to acquire the received code.

One advantage of sequential estimation over some of the other synchronization techniques is that it can achieve synchronization quickly. The sequential estimator has been demonstrated to achieve synchronization up to 23 times faster than the sliding correlator method. Acquisition times have been recorded from 90 ms at -6 dB, to 1 second at -12 dB signal to noise ratio, with white noise used as the interference signal (1:227).

Being vulnerable to interference is its greatest drawback. This is due to the demodulator working without the benefit of processing gain. Sequential estimation would work best in situations where the system contends with naturally occurring disturbances only (1:227).

Matched Filter Synchronizers

A matched filter generates a time reversed replica of the symbol it is matched to when an impulse is applied as its input. In the frequency domain, the transfer function of a matched filter is the complex conjugate of the Fourier transform of the signal to which it is matched. When all data bits are aligned, the filter output is at a maximum, or optimized. Anything other than total alignment, of the search area, results in a decreased output. This is called an optimal filter (1:229).

Both baseband and IF matched filters have been used, and for comparable filter lengths give similar results. IF matched filters are usually Surface Acoustic Wave (SAW) types. Baseband matched filters have been implemented with digital integrated circuits. The length of the SAW matched filters are limited by the base materials and losses in the devices themselves.

Digital baseband matched filters are limited by the ability to sum the correlated signal correctly, i.e. errors may appear in the exclusive-or circuits, and the electrical power dissipation of the integrated circuits themselves. Digital baseband matched filters use active circuits where

SAW matched filters use passive circuits. Figure 3 shows a baseband digital matched filter. In Figure 3 the digitized input signal is compared chip-by-chip, in this case twelve chips, to a stored reference signal by exclusive-or logic gates. In the AFIT system, the "stored reference" would actually be generated by the settings of the twelve switches on the front panel of each unit. The correlator generates a current output which is proportional to the degree of correlation between the reference and input signals. When the current output reaches a certain level, synchronization is said to have occurred.

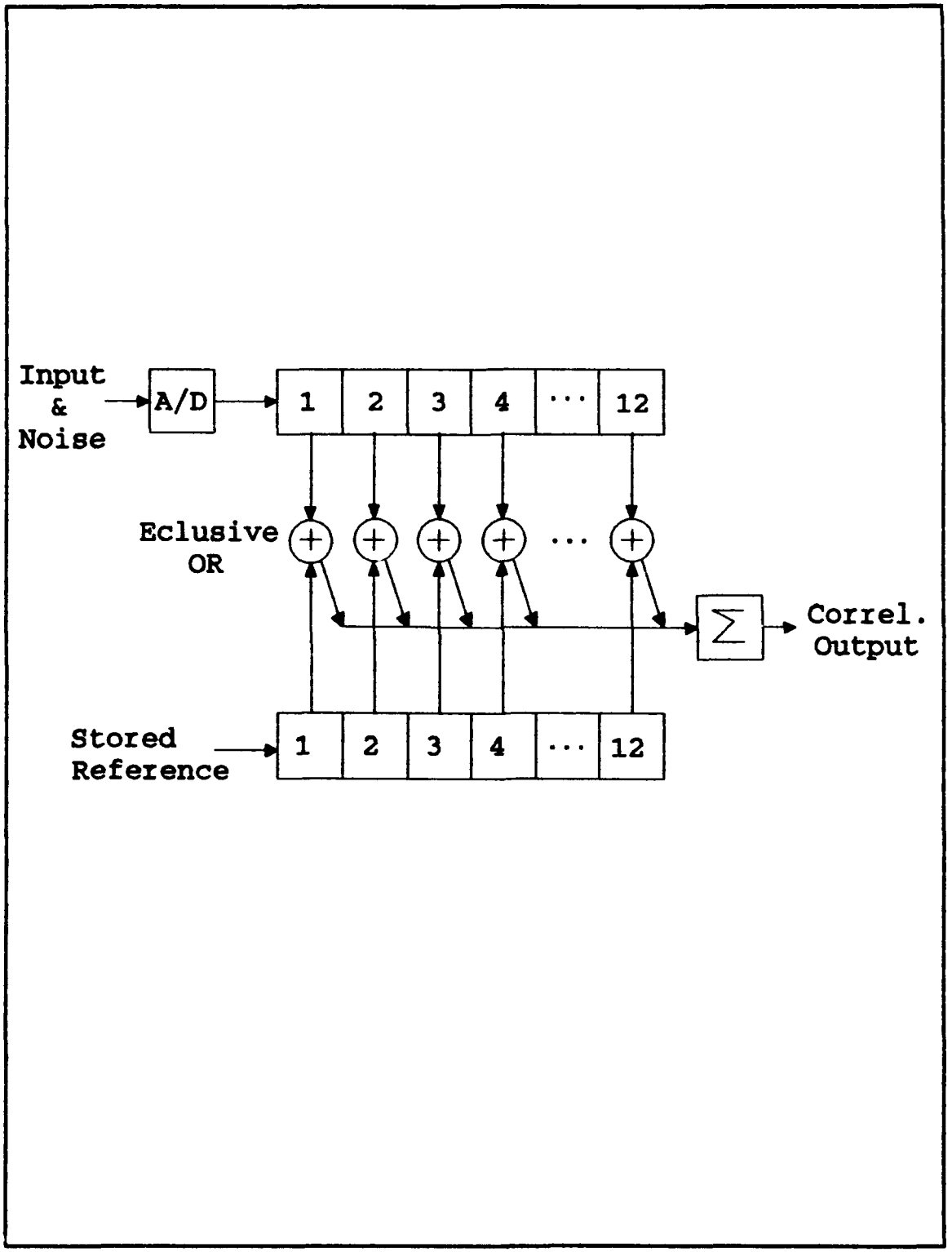

Figure 3. Baseband Digital Matched Filter.

Another type of matched filter is the delay line matched filter shown in Figure 4. The biggest drawback of the delay line matched filter is that it recognizes only one code sequence in particular, if the taps are not programmable. From Figure 4 one can see that the only way to achieve the maximum output is when the set of $\{T_1, T_2, T_5, T_7, T_8, T_{11}, T_{12}\}$ are summed and passed through an invertor, and the set of $\{T_3, T_4, T_6, T_9, T_{10}\}$ are summed and added with the first set. If the signal energy contained in each of the twelve delay elements is in phase, the output is twelve times greater than the unprocessed signal level. As seen here, only one particular code sequence will be capable of reaching the highest signal energy level. In Figure 4 this sequence, in binary, would be 001100101100.

One advantage of the delay line technique is the ability to enhance the signal by adding more delay stages in series. The available processing gain is (1:231),

$$G_p = 10 * \log(n) \qquad (1)$$

where (n) is the number of delay elements summed.

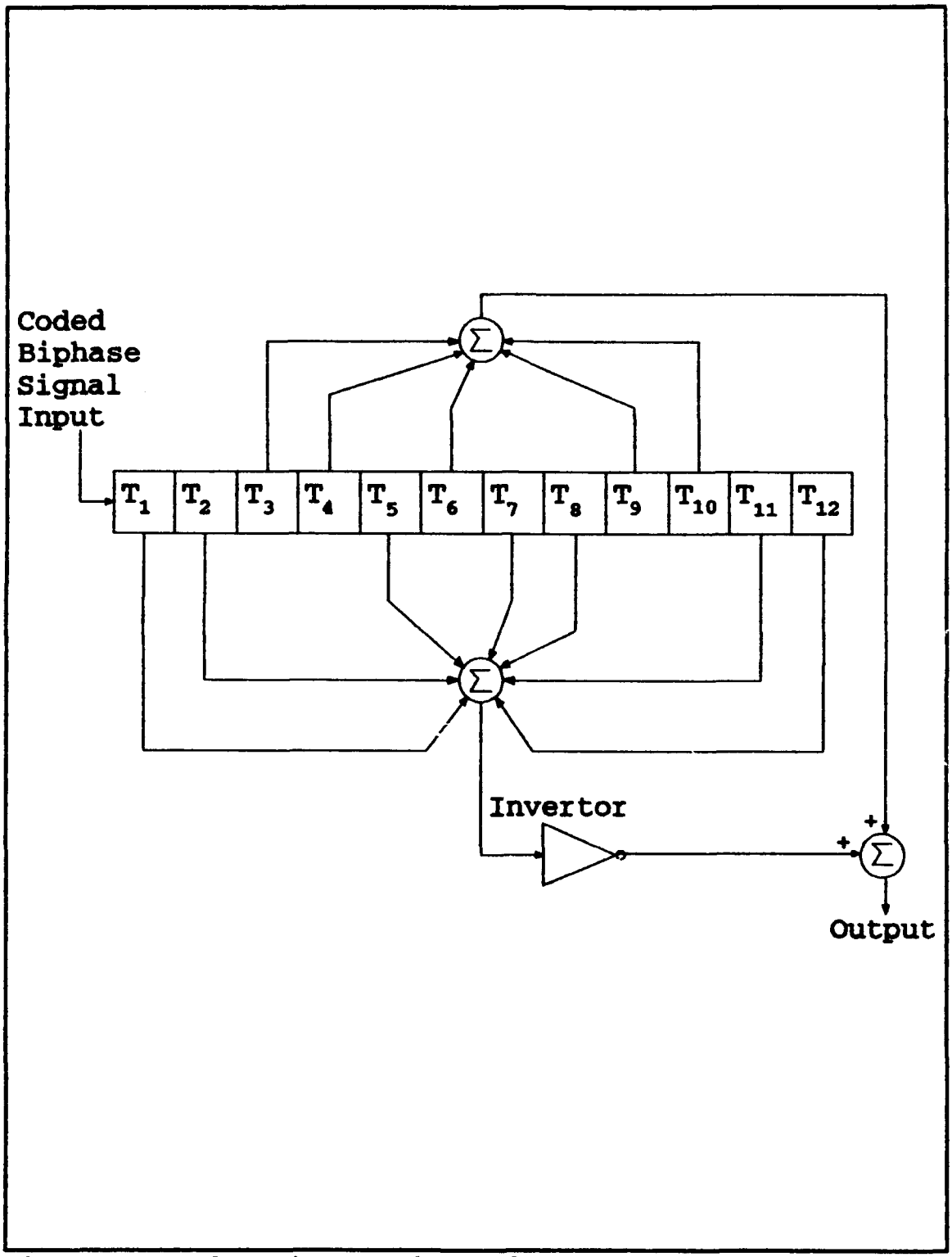

Figure 4. Delay Line Matched Filter.

There are limits to the maximum number of stages one can implement and still obtain synchronization. The practical limit of length in time is 20 to 40 ms which corresponds to a process gain of 40×10^{-6}/chip rate, or 33 dB for a 50 megachip per second code.

A significant point to consider when employing delay line matched filter synchronizers is that the code sequence clock period must be exactly duplicated or detection and synchronization will not occur. If it is not possible to ensure an accurate clock rate, an array of delay line matched filters with graduated delay periods must be used (1:229-232).

Luecke compares the acquisition times of DSSS systems using a type of matched filter, the code matched filter (CMF), and serial techniques. The CMF can search a large area of time-uncertainty in parallel thereby reducing the acquisition time by several orders of magnitude, as compared to serial search techniques. With the advent of parallel CMF detection schemes, two primary detection approaches have evolved. The first is threshold detection where the CMF results are compared to a set threshold, and the second is where the largest of the CMF outputs is assumed to reflect the correct code offset. Luecke introduces a hybrid

approach which attempts to take advantage of the best of both schemes. CMF schemes work well with large code uncertainties (5000 chips), but could also be used on small code systems such as the AFIT system (9:865-869).

Equivalent to the matched filters described earlier is the Surface Acoustic Wave (SAW) convolver. In operation, an input signal is inserted into one end of a piece of surface wave material and a reversed reference signal is inserted into the other end. The signals generate physical waves on the material which travel toward each other just like ripples on water. If the two waves (signals) are identical, the SAW material surface displacement caused by the waves is at a maximum. If the energy over the material surface can be integrated, the identical waves generate peak energy.

The signal wave has the PN code of the transmitter while the reference wave has the PN code of the receiver. A signal is generated from the waves of the material and is a function of the material motion. The physics of the device provide approximate integration of the energy of the surface wave displacement. The greater the correlation between the two signals, the larger the correlation peak. The peak is identical to the autocorrelation of the code sequence, but with half the period. Since the signals are traveling

toward each other, they align in half the time it would take for each generated wave to pass completely through the material. When each signal has completely entered the material, and before they start dissipating, half a period has elapsed and they are aligned.

Convolvers have been built with process gains (G_p) of 40 dB. They also have the advantage of operating at IF frequencies, which eliminates the need for baseband or A/D conversions. However they are limited in dynamic range and the receivers must have some way of restricting their input signal, such as an automatic gain control (1:232).

In a 1987 IEEE MILCOM letter by Eichinger and Kowatsch, a combination matched-filter/serial-search method is used to achieve synchronization in systems using code lengths much longer than the AFIT system. A matched filter, of the SAW convolver type, is used to process a short preamble code. The convolver provides a rough acquisition of the signal, which narrows down the search area for the serial search method to provide fine acquisition. This yields a considerable improvement over the serial search method in mean acquisition time (3:305-310).

Ormondroyd and Ravi, compared the matched filter to the serial search method and sequential estimation method. The matched filter synchronized more quickly for high signal-to-noise ratios, down to -15 dB, and the sequential detector had the best performance down to -25 dB and below (10:791-797).

Synchronous Oscillator

The synchronous oscillator (SO) is a free-running oscillator, oscillating at its natural frequency as long as no external signal is applied to it. When an external signal is applied, the SO attempts to track a sinusoidal component present in it. The SO can track, filter, frequency divide, and amplify the input carrier in a single process. Uzunoglu and White claim the SO has narrow-resolution bandwidth, high input-signal sensitivity, and fast acquisition properties, while its most unique feature is the functional bandwidth (16:516-517).

The narrow-resolution bandwidth of the SO is less than 1 kHz while the tracking range can extend over several hundred kilohertz. This allows the tracking of signals with -45 dB signal-to-noise ratios. With its high input-signal

sensitivity, the SO can track signals as low as -100 dBm (16:516-517).

Filtering properties are mainly determined by the resolution bandwidth of the SO while the tracking range is determined by the external signal level. They are independent and can be optimized separately.

A basic SO has a typical operational gain of 28 dB and the phase versus frequency characteristics give a tracking range of approximately 2 MHz (16:516-517).

Phase-locked Loop Description

A phase-locked loop (PLL) is an electronic circuit consisting of a phase comparator (detector), a low pass filter, and a voltage controlled oscillator (VCO). The VCO oscillates at a frequency proportional to the control signal applied to it. The VCO output frequency is applied to one input of the phase comparator. The output of the comparator is proportional to the difference between the input and VCO phases. The error voltage is filtered to attenuate high frequency noise components.

A normalized input signal will have the form

$$r(t) = \sin [\omega_0 t + p(t)] \qquad (2)$$

where: ω_0 is the nominal carrier frequency.

$p(t)$ is a slowly varying phase.

The normalized VCO output has the form

$$x(t) = 2 \cos[\omega_0 t + p'(t)] \qquad (3)$$

These signals produce an error signal at the phase comparator output which is of the form

$$\begin{aligned} e(t) = x(t)r(t) &= 2 \cos[\omega_0 t + p'(t)] \\ &\quad * \sin[\omega_0 t + p(t)] \\ &= \sin[p(t)-p'(t)] \\ &\quad + \sin[2\omega_0 t + p(t) + p'(t)] \end{aligned} \qquad (4)$$

It is assumed that the filter is low pass, which eliminates the second term on the right hand side of Equation (4). The error signal is then solely a function of the difference in phases between the input signal and the VCO output signal. This low pass assumption is a reasonable decision for loop

design (13:435). The error signal, e(t), is then used as the control signal for the VCO, which changes its output frequency in a direction to decrease this error. As the error decreases, the VCO frequency eventually equals the input frequency. When equal, the loop is phase-locked, or synchronized. Once the loop is locked, the low-pass filter limits the speed of the loop's ability to track the frequency changes at the input. During phase-lock, the VCO frequency exactly matches the input of the loop, except for a small phase error. This phase error generates the error voltage that changes the VCO frequency and keeps the loop locked. Figure 5 shows a phase-locked loop block diagram.

The loop equation has the form (13:435)

$$d\omega(t) = K\, e(t) * f(t)$$
$$= K\,[p(t) - p'(t)] * f(t) \qquad (5)$$

where: $d\omega(t)$ is the change in frequency.

K is the gain of the VCO.

* denotes convolution.

f(t) is the impulse response of the filter loop.

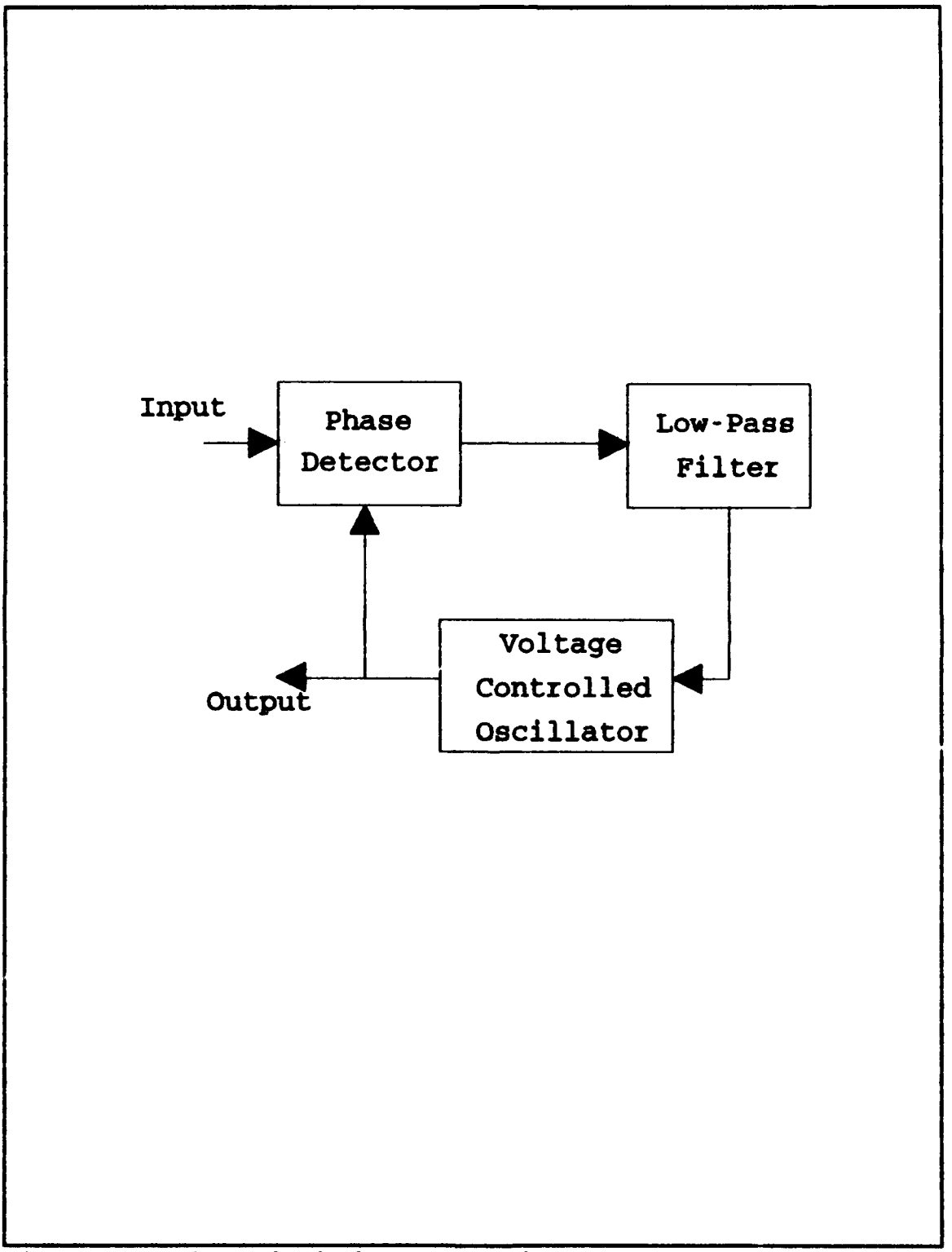

Figure 5. Phase-locked Loop (PLL).

The Fourier transform of Equation (5) is

$$j\omega\, P'(\omega) = K\,[P(\omega) - P'(\omega)]\,F(\omega) \qquad (6)$$

which can be rearranged as

$$P'(\omega) \,/\, P(\omega) = [K\,F(\omega)] \,/\, [j\omega + (K\,F(\omega))] = H(\omega) \qquad (7)$$

$H(\omega)$ is known as the closed loop transfer function of the PLL (13:436). The transfer function characterizes the steady state response to a sinusoidal input. The order of the PLL is the order of the highest order term in $j\omega$ in the denominator of $H(\omega)$. Equation (7) is of the first order for $F(\omega)$ = a constant. In practice, the majority of PLL designs are of the second order (13:439).

Both phase-locked loops and delay locked loops fall into the class known as correlation-loop architectures. A first order PLL is also known as a first order correlation loop. Kosbar examines minimizing the mean square tracking error of first order loops (8:156-160). He accomplishes this by varying the locally generated cross correlation function produced by the voltage controlled oscillator. Filtering a replica of the original transmitted signal generates an optimum cross correlation waveform. This

filtering imposes a 90 degree phase shift, with respect to the incoming signal, at all frequencies. The amplitude response is a function of channel signal to noise ratio. When the transmitted signal is sinusoidal, as in the AFIT system, analysis indicates the optimal loop is the conventional PLL.

Summary

Synchronization is the most difficult aspect of a spread spectrum system. This chapter described several synchronization methods including the baseband matched filter, delay line matched filter, convolver, sliding correlator, transmitted reference, sequential estimation, and the synchronous oscillator. Several articles dealing with these synchronization methods were also reviewed. This chapter also included a description of the phase-locked loop and review of an article dealing with first order correlation loops.

III. Phase-Locked Loops

The phase-locked loop (PLL) is used for both the acquisition and tracking of a signal. In this thesis the emphasis will be on tracking since several means of acquisition have been described in the previous chapter. Several PLL circuits are described in this chapter. A combination of one of the earlier described acquisition methods and a PLL circuit for tracking, would improve the AFIT DSSS system's performance. A selection of the PLL IC to be used in a modification of the AFIT system is made in this chapter.

PLL Implementation

At an IF frequency of 21.4 MHz, a phase-locked loop could be easily installed in the receiver and the performance of the system evaluated (14:124). A possible configuration of such a modification is shown in Figure 6. With a PLL in the receiver, it would be a much simpler task to evaluate the actual performance of some of the synchronization techniques described in this thesis.

Oscillator drift would be negated by the tracking ability of a PLL.

In Figure 6, the DSSS input signal at 446.0 MHz is mixed with an internally generated signal of 424.6 MHz. The difference between the input and internally generated signals, 21.4 MHz, will be bandpass filtered to attenuate unwanted signal components and limit noise. After filtering, the input signal is mixed with the code from the VCO driven PN code generator. The resulting error signal drives the PLL to a "locked" condition. The despread signal is then routed to the demodulator. The 21.4 MHz IF frequency is one at which a broad range of PLL circuits could effectively operate.

PLL Integrated Circuits

There are many PLL integrated circuits (ICs) that could be used on the DSSS system described here. All of the ICs examined contain the bandpass filter, phase comparator, and VCO on a single chip. It is also possible to custom design a PLL circuit using a specific VCO chip, a particular filter chip, and a desired phase comparator chip.

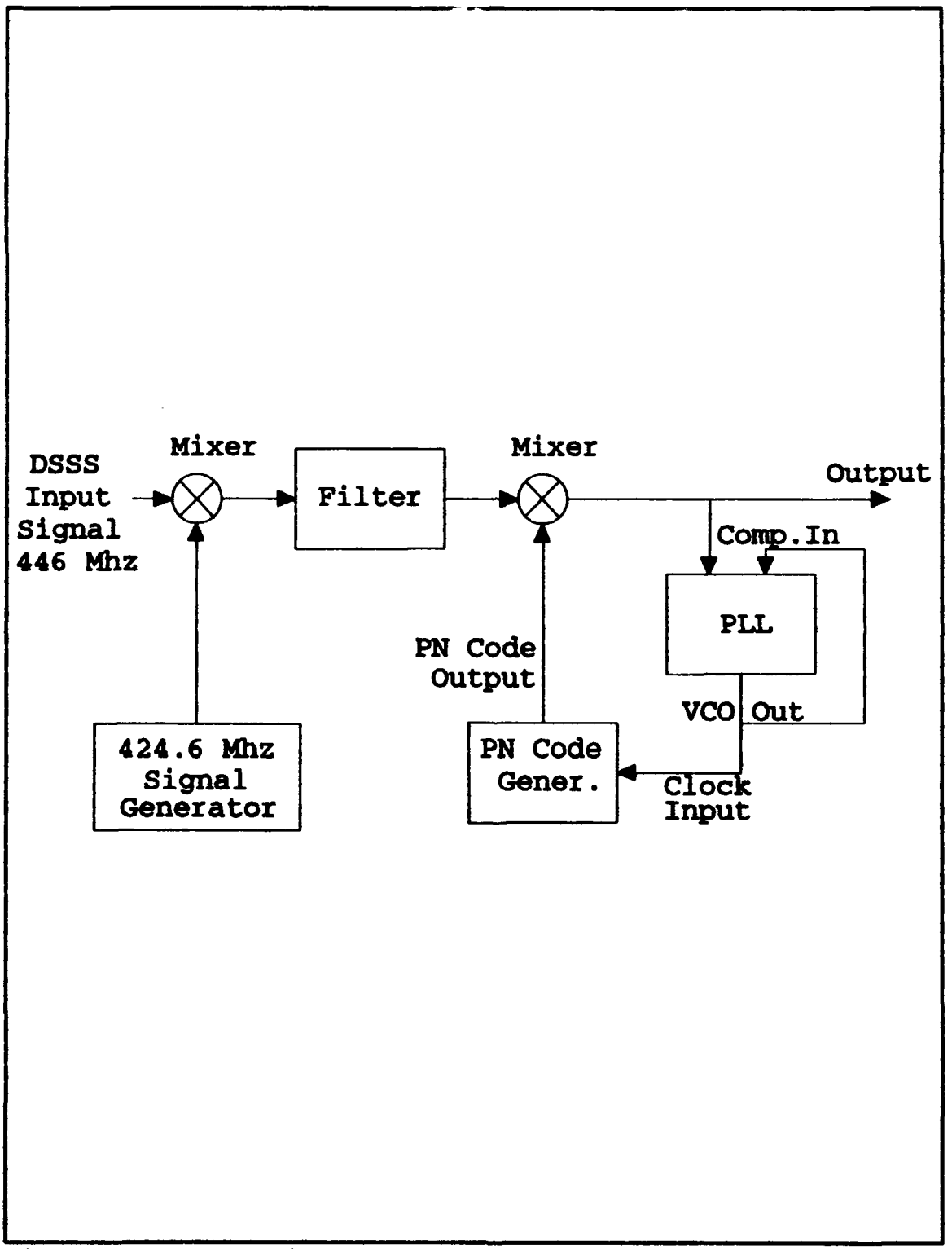

Figure 6. PLL Implementation in a DSSS Receiver.

The Signetics NE560B is a signal conditioner-demodulator and has a useful range of 1 Hz to over 30 MHz. Tracking range of the chip is externally adjustable from +/-1% to +/-15% of the free running VCO frequency. Maximum operating frequency is well within range of the suggested IF frequency of 21.4 MHz. The free running frequency of the VCO is set by the selection of an external capacitor and can be fine tuned by the addition of a potentiometer. The NE560B can achieve signal lock on an input signal as small as 100 µvolts (6:B-3).

A PLL circuit with the same parameters is the NE562B. This IC has two sets of differential inputs. One input for the FM/RF signal and the other for the phase comparator local oscillator input. Both sets of inputs can be used in a single-ended or differential mode. An internally regulated voltage source is provided to bias the local oscillator inputs of the phase comparator. The VCO has dual outputs and can be used to drive logic circuits in synchronization applications, such as the shift registers in a matched filter. The NE562B can achieve signal lock on an input signal as small as 200 µvolts (6:B-13).

A PLL integrated circuit designed for operation up to 50 MHz is the Signetics NE564B. It is used in high speed

modems, FSK transmitters and receivers, and frequency synthesizers. It does not need elaborate signal filtering circuits for FSK applications, and can operate from a single 5 volt supply (6:B-19).

The thermal drift rate of the VCOs in the above PLL ICs is less than 0.5% for a 10 degree C change. This makes them stable oscillators, which is advantageous in the tracking process once acquisition has been achieved.

PLL Selection

The Signetics NE560B, NE562B, and NE564B Phase-lock Loop integrated circuits were examined in this thesis for operating parameters that would be compatible with the DSSS system. With an operating frequency range of 0.1 Hz to over 30 MHz, required supply voltage of 14 volts at 12 ma (plus or minus 2 volts), a dynamic range of 80 dB, and minimum input signal level of 200 μvolts for frequency lock, the recommended PLL IC for implementation is the NE562B.

Summary

This chapter gave brief descriptions of several phase-locked loop integrated circuits. Also the possible improvements a PLL could make to the AFIT DSSS system are given. A selection of the PLL IC to be used in the AFIT DSSS system modification is also given in this chapter.

IV. Theory

Analysis of synchronization times and bit-error rate, for the synchronization methods evaluated, are discussed in this chapter. For the mathematical equations used to model the system transmitter and receiver see Stephens thesis (14).

Synchronization Times

The DSSS system uses an FM exciter with a crystal oscillator clock running at a frequency of 12.388 MHz. This clock signal is routed through two frequency multiplier circuits, X3 each, to increase the clock frequency to 111.49 MHz. This signal is divided in frequency by 40 to develop the 2.78725 MHz PN code generator clock signal. The 111.49 MHz signal is also frequency multiplied by four to generate the 446 MHz signal used for the carrier (14:55). The code sequence has 127 chips.

From the PN clock chip time of 358.74 ns, (1/2.78725 MHz), a code period of 45.56 μs per sequence (127 chips * 358.74 ns) is achieved (14:50). Each code

chip contains 160 cycles of the 446 MHz carrier signal (14:59). There are 21,950 (1/45.56 µs) code sequences transmitted per second. The average time of synchronization found in the tests run by Stephens was 164.1 ms (14:105). This corresponds to 3601.8 sequences received (164.1 ms / 45.56 µs) before synchronization occurred.

In order to transmit the digital data over this system some number of chips-per-bit must be used. 127 chips-per-bit is a reasonable choice given the polynomial 7 degree of the code sequence. This choice could be easily implemented with the system in existence.

It should be noted that the synchronization times measured in Stephens' work take into account both the code sequence synchronization and the carrier synchronization. Carrier synchronization is defined here as the demodulation of the incoming signal, after code synchronization. There could be hundreds of code sequences received after code sequence synchronization and before carrier synchronization, but there is no way to separate their times without making modifications to the receiver. While this number of sequences cannot be counted, some of the propagation delay present in the test set-up can be eliminated. The set-up used to measure synchronization times would theoretically

have the largest propagation delay between the DSSS audio output and the HP5326A Interval Timer stop input jack.

Figure 7 illustrates how to connect a dual trace oscilloscope to the test set-up in order to measure the time delay of passing the interval timer stop pulse signal through the FSK demodulator.

By synchronizing the oscilloscope with the signal at input 1 and using a delaying time base with the oscilloscope, the propagation delay of the stop signal could be accurately measured. This value could then be subtracted from the synchronization times of Stephens' (14:105). It would be worthwhile to rerun the synchronization time test, with the oscilloscope in the set-up, simply to recheck the times. Measuring the delay through the FSK demodulator would help increase the precision of the readings obtained.

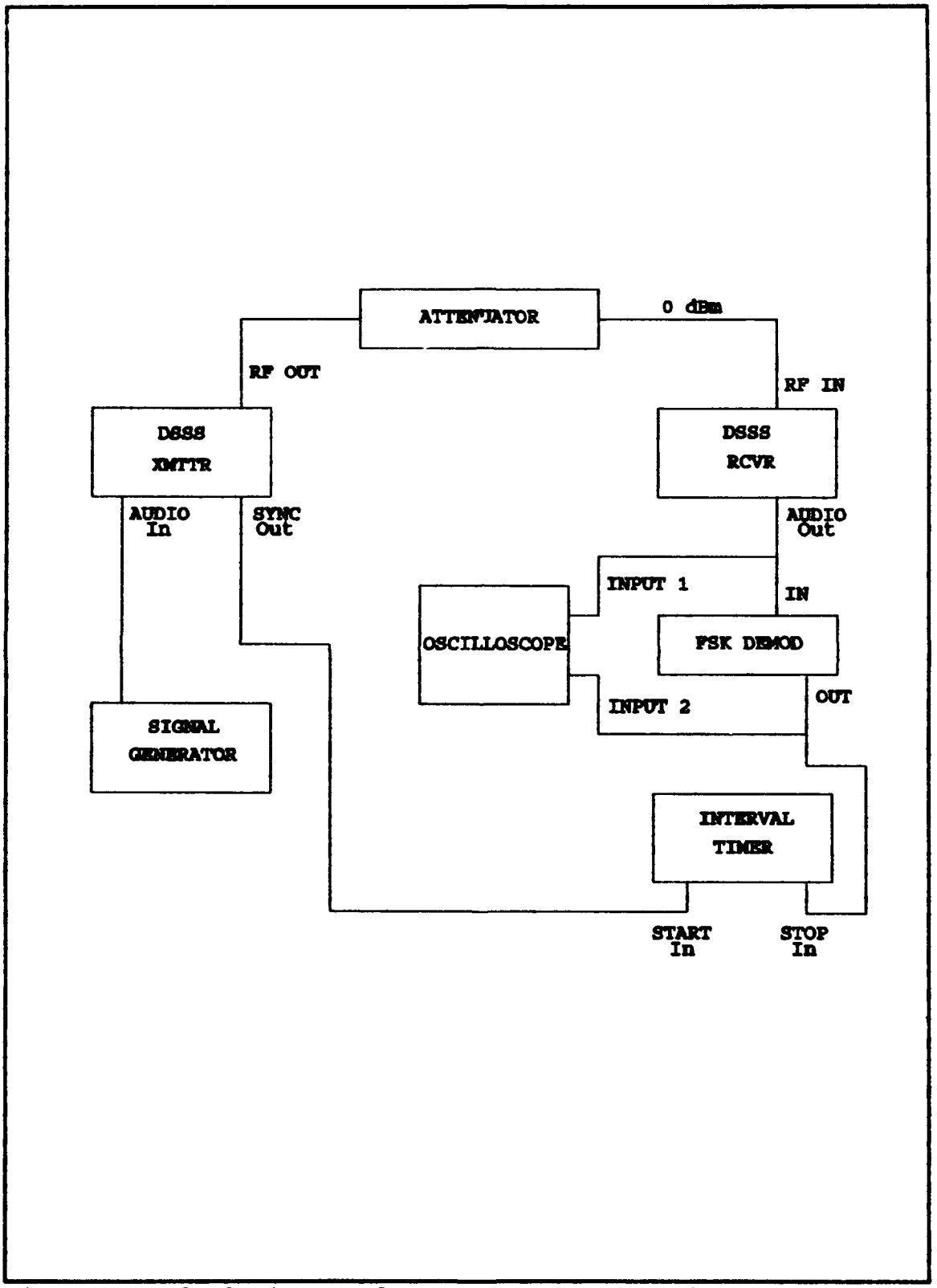

Figure 7. Block Diagram for Synchronization Time Measurement.

The quickest possible synchronization time, of Stephens' synchronous oscillator, would occur when the received PN code sequence matches the receivers' PN code generator sequence exactly, from the moment the two signals were compared, or mixed, in the receiver. If the first chip to enter the receiver and be compared was identical to the first chip of the receivers code sequence, synchronization will occur in the time necessary for one sequence to be compared. This would be approximately 45.56 μs and corresponds to the fastest theoretical code sequence synchronization time (127 chips * 358.74 ns).

If the first chip to be compared in the receiver is the second chip in the sequence, it would be necessary for one chip duration less than two complete sequences to be compared before synchronization could occur. The comparison process takes the first chip received and compares it to the first chip of the receivers' code sequence generator output. The process continues until all chips in the sequence have been compared. This could be thought of as the shortest, maximum synchronization time possible. The time needed for synchronization would be approximately 90.76 μs (127 chips * 358.74 ns) + (126 chips * 358.74 ns).

Both of these cases assume the code sequences will have

no errors and will synchronize on the first pass through a complete code sequence. In practice this will not happen often due to noise induced chip errors.

Sliding Correlator Synchronization Time. The DSSS system built by Stephens has a baseband bandwidth of 4 kHz (14:107). Applying the rise time-to-bandwidth relationship T_R=0.35/BW, synchronization could be achieved in as little as 87.5 μs (1:21). It is assumed the PN code period fits in the bandwidth used. This is the ideal situation where the chips of the received signal and the generator align exactly as the signals are initially compared. A more realistic minimum synchronization time is obtained by assuming the incoming signal will pass through at least 128 chips prior to synchronization occurring. If the first incoming chip to be compared does not match that of the generator, the remaining chips in that sequence will need to passed through before a new sequence begins. This would extend the synchronization time to twice the realistic minimum, or longer.

Transmitted Reference Synchronization Time. This method enjoys the advantage of almost instantaneous synchronization. However, the military needs communication systems that exhibit anti-jam and low probability of

intercept characteristics. A transmitted reference method cannot accomplish that alone. If interference or jamming were a threat, another form of synchronization would be necessary after initial synchronization by transmitted reference.

Sequential Estimation Synchronization Time. In this technique the receiver to be synchronized must have the ability to demodulate the incoming signal to extract the data chips. For a 2^n-1 length PN code, demodulated chips are loaded into the n stage sequence generator which is then started with this initial fill. Once the local code generator is loaded with the demodulated data it must search ahead by a number of chips determined by the formula (1:227)

$$n + T_p / f_K \qquad (8)$$

where: n is the chips per code length, 127 chips.

T_p is receiver processing delay, assume 100 ms.

f_K is the code clock rate, 2.78725 MHz.

100 ms is assumed as the processing delay because the time for synchronization of the AFIT system with the SO is 164.1 ms and the theoretical synchronization time of the SO is 106.1 µs. It is assumed most of the difference between

these times is processing delay.

T_p / f_K will be small compared to n, which makes the search ahead 127 chips. With 127 chips and each chip being 358.74 ns in duration, the time to synchronize is 45.56 µs. This method demodulates the signal without benefit of processing gain and is susceptible to interfering signals and noise sources.

Matched Filter Synchronization Time. Each delay element of the delay line matched filter has a delay equal to the period of the code clock. Therefore each element contains energy equal to only one code chip at one time (see Figure 4). With 127 chips and a 2.7875 megachips/sec clock rate, (358.74 ns), the synchronization time is 45.56 µs, (127 chips * 358.74 ns). This assumes no errors are present on the incoming coded signal.

The baseband digital matched filter uses an input shift register and stored reference shift register. Once the stored reference is inserted into its shift register, which could be all its chips at one time, the input signal is clocked into its shift register. The input signal is inserted one chip at a time (see Figure 3). With 127 chips and a clock period of 358.74 ns the minimum theoretical

synch time is again 45.56 μs. This assumes all chips in the input shift register match the chips in the reference shift register after 127 clock pulses. Synchronization time for the delay line and baseband matched filter type could be approximately equal.

Another type of matched filter is the convolver. The convolver employs the reference signal and the incoming signal being applied to opposite ends of a surface wave material. One signal is modulated by a code, usually the transmitted signal, and the other by the codes mirror image, usually the reference signal. These signals generate a maximum correlation peak at some point as they propagate in opposite directions across the material. This peak is identical in shape to the autocorrelation of the code but with half the period. The synchronization time would be, 127 chips * 358.74 ns, or 45.56 μs. This method has the disadvantage of needing its input signal restricted in some way, such as an automatic gain control circuit, in order to keep from damaging the surface wave material.

Synchronous Oscillator. The acquisition time of a synchronous oscillator can be estimated from its natural frequency (17:1220). With the tracking range of the oscillator known, the equation $1/(\pi * f_o)$, where f_o is the

frequency tracking range, gives the acquisition time (17:1220). The natural frequency of the synchronous oscillator in the current system is 111.5 MHz. It is divided by 40 to obtain the 2.7875 MHz clock frequency. The receiver clock frequency obtained from the synchronous oscillator is used to achieve lock.

The synchronous oscillator in use should be able to achieve lock at frequencies from 2.7860 MHz to 2.7890 MHz. This gives a tracking range of 3 kHz. Inserting these numbers into the equation above gives a theoretical synchronization time of approximately 106.1 μs. Working backwards from the 164.1 ms synchronization times measured by Stephens, a tracking range of 2 Hz is calculated. This could be too small a range to be the actual tracking range of the oscillator. This indicates that part of the difference between the theoretical and measured synchronization times must be the carrier synchronization time and propagation delay discussed earlier in this thesis.

Bit Error Rates

For the bit-error rate test conducted by Stephens on the DSSS system, a non-coherently detected FSK signal at

300 bits-per-second was used. Noncoherent indicates that no signal phase information is used or needed for information (data) recovery. The two frequencies used for the FSK signal were 2025 Hz and 2225 Hz. A PN sequence with a length of 65,535 bits was used to ensure randomness of ones and zeros, or highs and lows was achieved (14:111).

The equation for probability of bit error for a noncoherently detected FSK signal is (13:164)

$$P_B = 1/2 \exp(-E_b / 2N_0) \quad (9)$$

where: E_b is the energy per bit.

N_0 is noise power spectral density level (Watts/Hz).

Equation (9) corresponds to the theoretical curve of bit-error rate versus E_b/N_0 ratio referenced in Stephens thesis. In reading Stephens' work and comparing the theoretical curve to the measured bit-error rate, it was noted that the two curves were similar in shape. However, poor receiver sensitivity caused a difference between the curves of approximately 30 dB (14:112-114). Remeasuring the P_b versus E_b/N_0 with PLL as part of the synchronization method is highly recommended.

The error performance depends on the bandpass filter bandwidth. The probability of bit error decreases as the bandwidth decreases. However, the minimum bandwidth allowed is of course the Nyquist rate, which is the smallest allowed bandwidth without introducing intersymbol interference. The probability of bit error equation using signal amplitude and bandwidth information is (13:163)

$$P_B = 1/2 \exp (-A^2 /(4 N_0 W_f)) \quad (10)$$

where: A is signal amplitude.

W_f is the filter bandwidth.

N_0 is the noise power spectral density level.

which becomes

$$P_B = 1/2 \exp (-E_b / 2N_0) \quad (11)$$

as $T = 1/W_f$ and $(1/2\ A^2\ T)$ equates to the energy per bit E_b. As shown by equations (10) and (11), as the bandwidth decreases E_b/N_0 increases causing the probability of bit error to decrease.

Summary

This chapter found theoretical synchronization times and a bit-error rate for selected synchronization methods. The synchronization times assume synchronization occurs on the first pass through the sequence, using all 127 chips. Where possible, equations were used to assist in the evaluation.

The theoretical synchronization times are:

Stephens' SO	45.56 μs
Sliding Correlator	87.50 μs
Transmitted Reference	instantaneous
Sequential Estimation	45.56 μs
Delay Line Matched Filter	45.56 μs
Baseband Matched Filter	45.56 μs
Convolver Matched Filter	45.56 μs
Uzunoglu's SO	106.1 μs

The probability of bit-error is found the same way for all noncoherently detected FSK signals. It is found using the formula in Equation (9).

V. Comparisons

This chapter contains a comparison of the methods of synchronization evaluated, and selection of the method that shows the promise of best operation if implemented. Bit-error rate and synchronization times were evaluated in earlier chapters.

Synchronization Comparisons

The sliding correlator has the advantage of being simple in design, but for code sequences of considerable length it is not practical to check the total number of code-phase positions due to circuit time constraints. Any code sequence used for military applications would be of considerable length. This method would be of little use.

The transmitted reference method allows the building of smaller, lighter, cheaper receivers, clearly advantageous for military purposes. This method has severe problems with interference and jamming of signals. Therefore this method is undesirable for military applications.

Sequential estimation can achieve synchronization very quickly, but has the same drawbacks with susceptibility to jamming. It is not recommended for military applications where security or reliability is required.

A baseband matched filter provides the characteristics of synchronization time and bit-error rates desired for this system. The ability to change the stored reference of the receiver, using the PN code generator switches, make this an adaptable method desirable for military purposes. The drawback of this method is the need to add an additional stage to the receiver to bring the signal back down to baseband.

The delay line matched filter has the ability to increase processing gain by adding more filter stages in series. There is a limit to the number of stages that can be added, due to processing time. A means of changing the stored reference code would need to be added to this method to be practical for military applications.

Another type of matched filter is the Surface Acoustic Wave (SAW) convolver. The three matched filter methods provided the fastest theoretical synchronization times of the methods evaluated. The disadvantage of restricting the

input signal power level to the convolver is not a problem here. This method could be implemented with an IC and should work well in this system.

The synchronous oscillator (SO) in this system proved itself capable of synchronizing quickly and tracking the signal in low signal-to-noise ratios. A theoretical synchronization time of 45.56 μs was computed for this method. Stephens' experiment yielded an average synchronization time of 164.1 ms. The theoretical synchronization time for an SO from Uzunoglu's letter was calculated earlier to be approximately 106.1 μs. The problem is the time delay between synchronization and the stopping of the interval timer. The synchronization times recorded by Stephens may have excessive propagation delays in them, and the operation of the SO could be much faster than measured.

Bit-error Rate

The bit-error rate is more a function of the system detection method than any other parameter. No one synchronization method evaluated here could provide a discernible advantage in bit-error rate over the others.

Summary

No one synchronization method proved advantageous over the others based on synchronization time alone. Other factors must be taken into account in order to make a recommendation as to which method should be implemented in the AFIT DSSS system. Based on this, the matched filter convolver is recommended for implementation in the AFIT DSSS system. The bit-error rate is the same for all the synchronization methods evaluated. It is determined by the system and not the synchronization method.

VI. AFIT System Modification.

In this chapter will be information on selecting the value of capacitors for PLL ICs to enable a phase-locked loop to operate with the AFIT DSSS system. A PLL IC was recommended in Chapter III for help in code synchronization, and the information needed for installing it in the DSSS system is included here.

The PLL ICs described in a Chapter III all have manufacturers data sheets to assist in the selection of the capacitors and resistors needed for the operating parameters desired. These include the free-running VCO frequency, range of frequency tracking, and low pass loop filter.

Free Running Frequency

Figure 8 is a chart from Signetics, used to determine the free-running frequency of the VCO for the Signetics NE560B and NE562B (6:B-6). This corresponds to a range of frequencies from 500 Hz to 50 MHz. To provide the free-running frequency equal to the IF of 21.4 MHz, the capacitance value found from Figure 8 is approximately 20 pF

for the Signetics NE560B and the NE562B. This value may not be the exact capacitance needed, but should enable either of the two PLL circuits listed above to operate. Some fine tuning of capacitance values, by experimentation, would be a task for future work.

Input signals greater than 4 millivolts provide the PLL the ability to track the input signal frequency over a range of 20%. In this case, it is a range of 4.28 MHz. Input signals as small as 1 millivolt provide a 10% tracking range, or 2.14 MHz (6:B-11).

The Signetics NE564B has a manufacturer's chart to select the proper capacitance value for a desired frequency. It also comes with an equation for determining the capacitance needed. This equation was not given with the NE560B and NE562B.

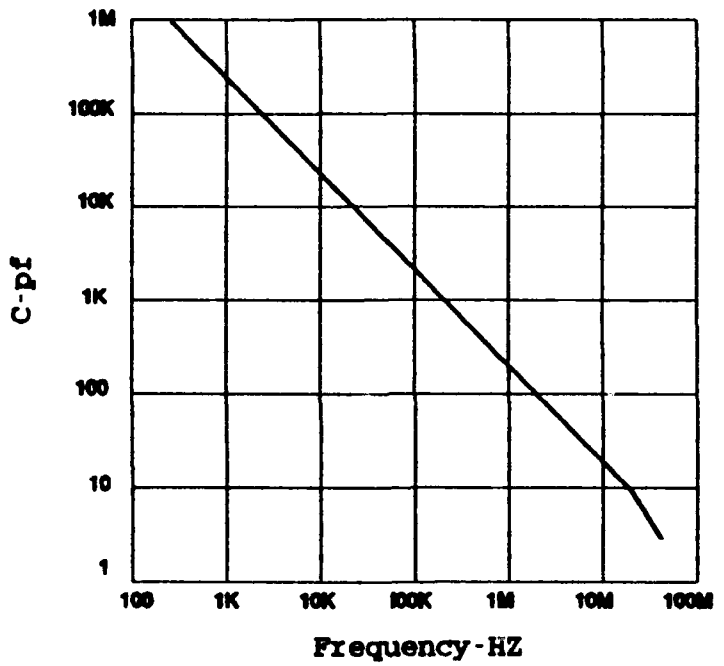

Figure 8. Free Running Oscillator Frequency as a Function of VCO Timing Capacitance.

The free running frequency of the NE564B can be found from the following equation (6:B-20)

$$f = 1 / (16 * R * C) \qquad (12)$$

where: f is the desired frequency, in hertz.
R is the resistance in ohms, typically 100 ohms.
C is the capacitance value, in Farads.

Inserting the desired frequency of 21.4 MHz and the given resistance of 100 ohms into equation (12), and solving for the capacitance value, 29.2 pF is obtained. This is close to the value derived from the chart for the NE560B and NE562B, and is the value recommended for implementing a phase-locked loop in this DSSS system.

Loop Low Pass Filter

Figure 9 gives a representation of the equivalent circuit for the loop low pass filter of the Signetics NE560B. The error signal from the comparator passes through the filter, and all undesired components of that signal are attenuated, part of which is noise from the received signal.

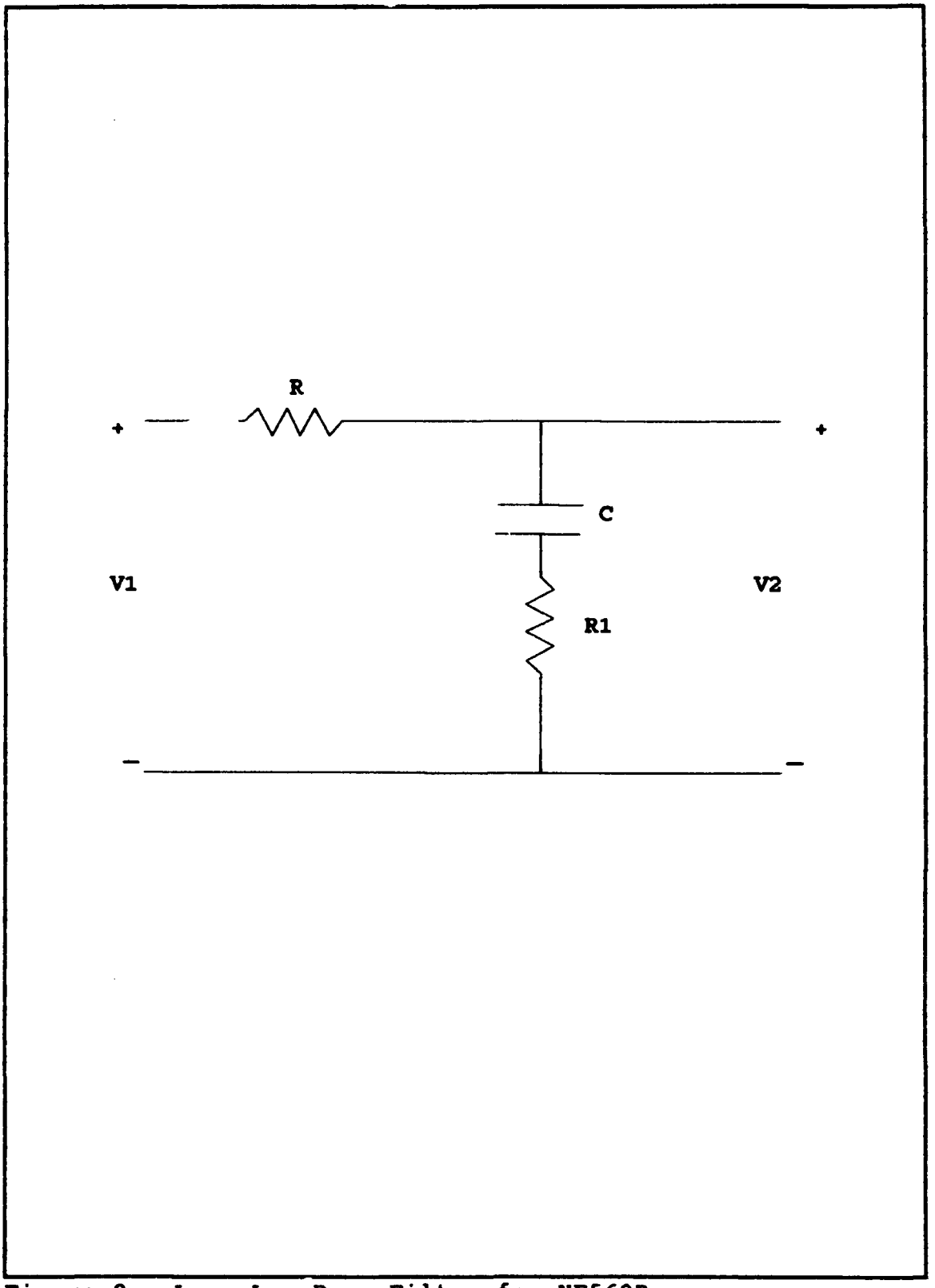

Figure 9. Loop Low Pass Filter for NE560B.

The filter transfer characteristic corresponding to the circuit of Figure 9 is (6:B-7)

$$V_2(s)/V_1(s) = (1 + s R_1 C) / (1 + s (R_1 + R) C) \qquad (13)$$

where: s is the complex frequency variable.

R is the impedance seen looking into the loop low pass filter pins of the IC, 6000 ohms.

R_1 is a resistance in ohms, designer selected.

$V_1(s)$ is the Laplace transform of the input.

$V_2(s)$ is the Laplace transform of the output.

C is a capacitor in Farads, designer selected.

Figure 10 is the equivalent circuit for the loop low pass filter of the Signetics NE562B. The corresponding filter transfer characteristic is the same as the NE560B. The L1 and L2 points are connections to the loop low pass filter pins of the IC (6:B-18).

A low pass filter is used to set the loop response time, controlling the capture range and rejection of out of bandwidth information. At frequencies greater than 5 MHz the filter helps ensure loop stability (6:B-18).

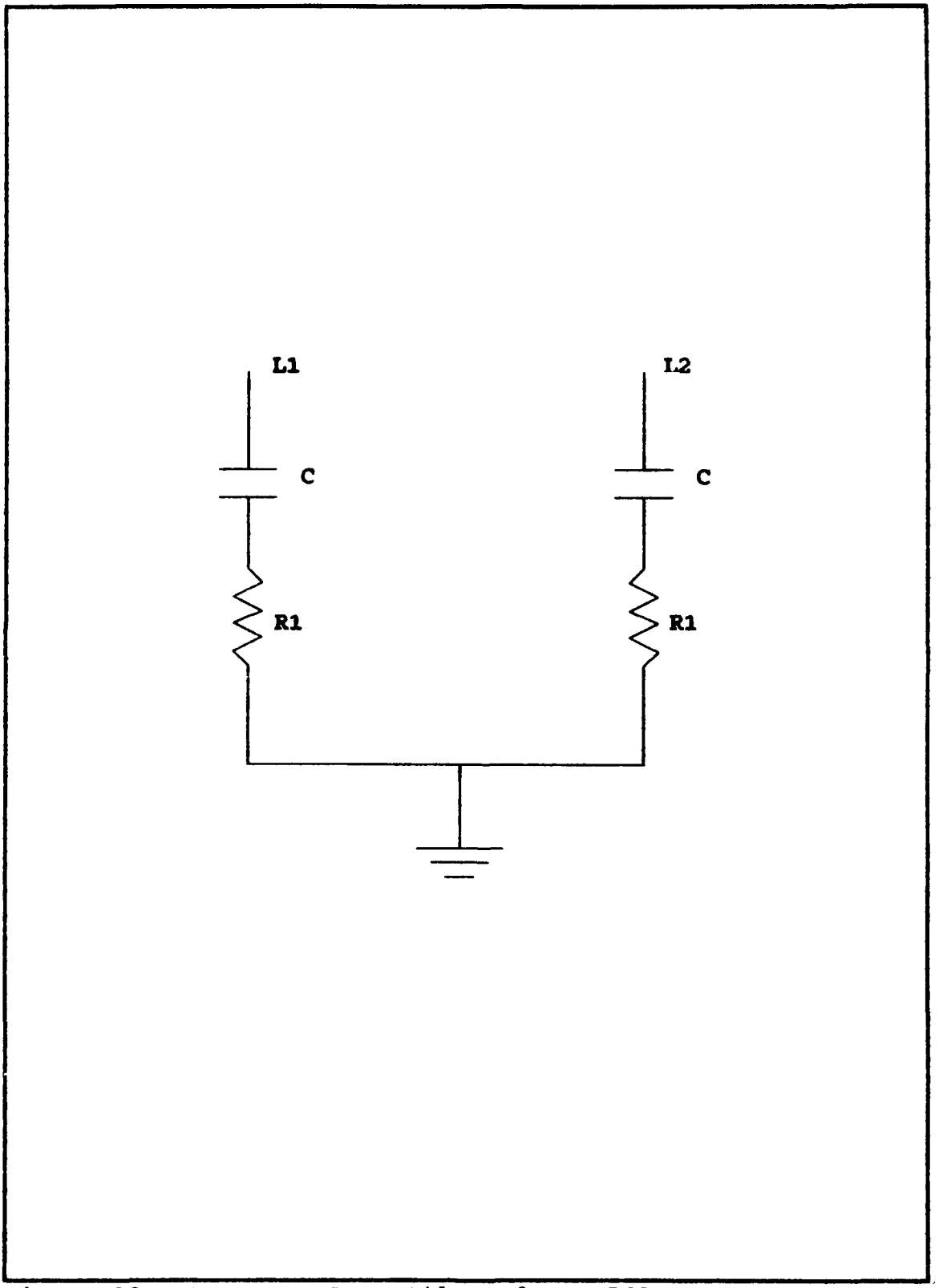

Figure 10. Loop Low Pass Filter for NE562B.

PLL Installation

Figure 11 is a block diagram of the NE562B with the pin numbers of the integrated circuit included. The pages following Figure 11 are a listing of the connections to be made between the DSSS system and the NE562B. The Kesteloot article schematic diagram was used to identify the connecting points of the inputs and outputs from the doubly balanced mixer and the PLL.

Figure 12 is a block diagram showing the signal connection points to install a PLL in the AFIT DSSS system. The junction points correspond to connections in the Kesteloot article schematics. It is recommended that anyone attempting work on this system in the future have a copy of the Kesteloot article as a reference for that work.

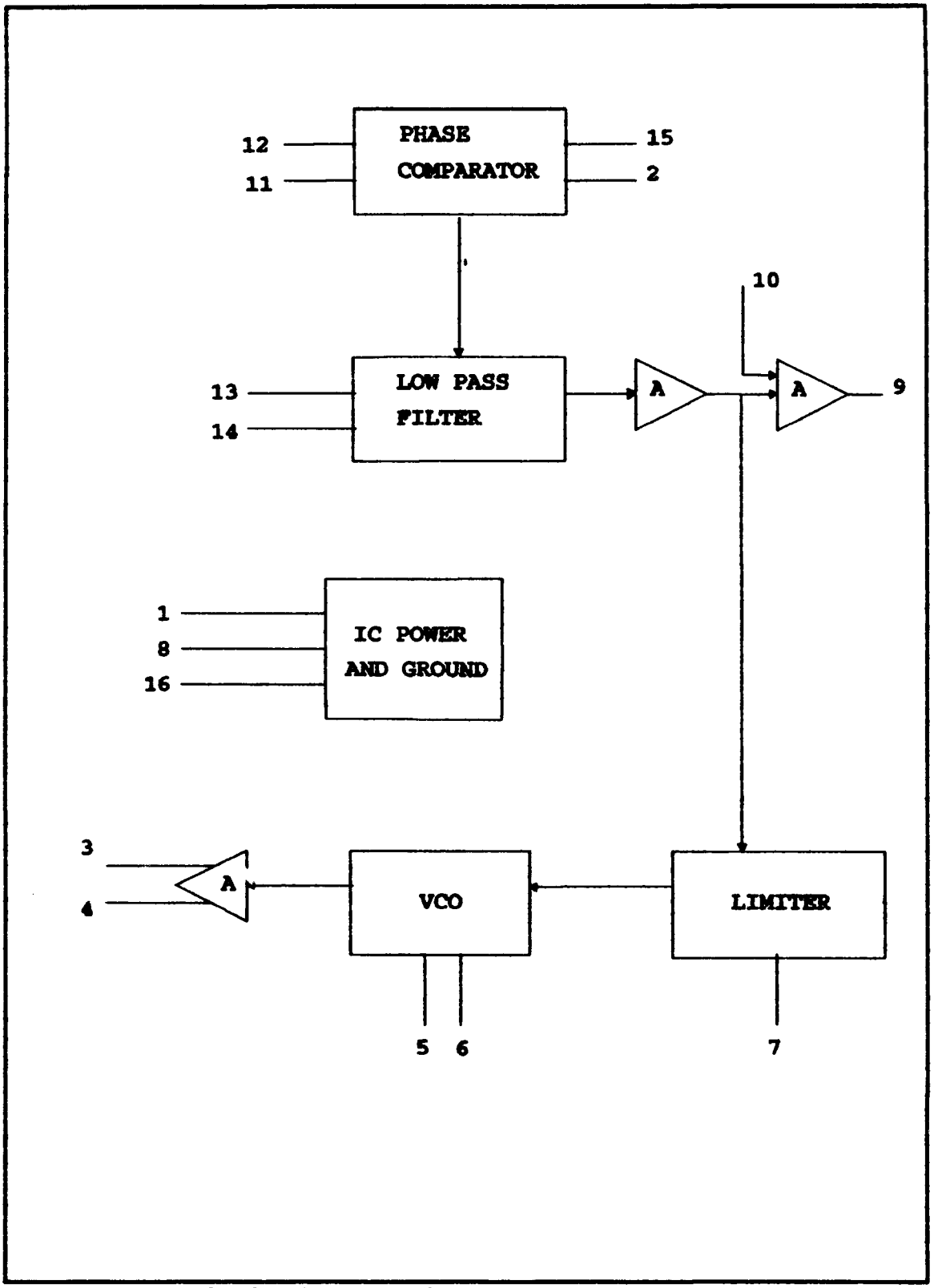

Figure 11. Block Diagram of PLL IC NE562B.

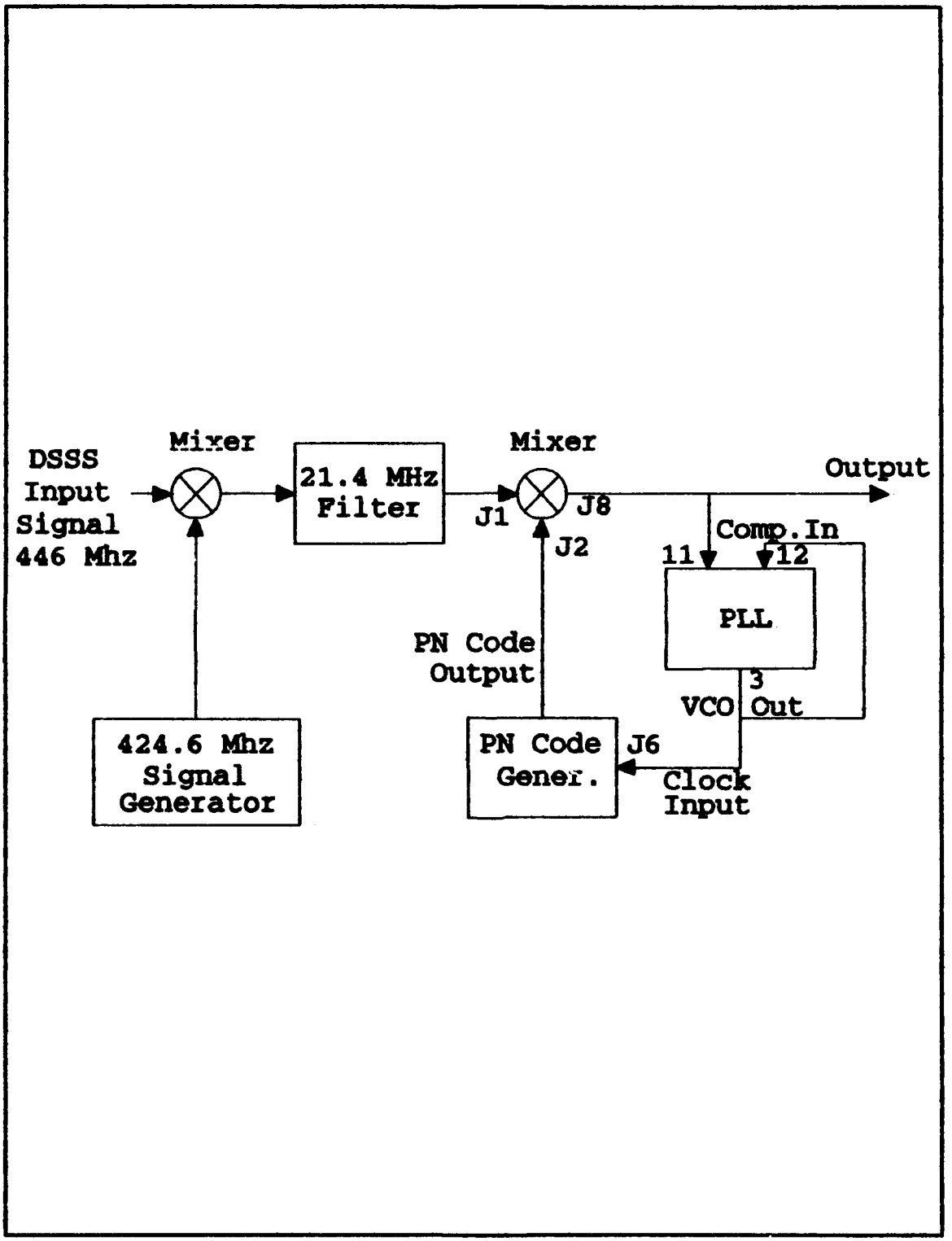

Figure 12. Block Diagram of the Installation of a PLL in the AFIT DSSS System.

NE562B Pin Connections

Pin	Connection
1	An internally regulated bias reference voltage source used to provide bias current to the phase comparator input terminals, pins 2 and 15. A 1000 ohm resistor is to be connected between pins 1 and 2, and another between pins 1 and 15. A 0.1 µF capacitor is also to be connected from pin 1 to circuit ground.
2	One of the two differential inputs to the phase comparator, the other is pin 15. This circuit is not being used in the differential mode, and the inputs are biased as described in pin 1 connections.
3	VCO output 1 which is fed to the Doubly Balanced Mixer PN input, J6, in the Kesteloot article diagram. It is also fed to the phase comparator FM/RF input 2, which is pin 12.
4	VCO output 2 which is a 180 degree shifted version of the signal at VCO output 1. For proper VCO output amplifier operation this pin needs to be connected through a 12000 ohm resistor to ground.
5	The timing capacitor connected between pins 5 & 6 sets the free running frequency of the VCO. It is recommended that a variable capacitor be installed across these terminals, having a range of capacitance of approximately 1 to 50 pF. A value of 20 pF was obtained from the Figure 8 chart to set the free running frequency to 21.4 MHz.
6	See pin 5 connection.
7	The tracking range of the PLL is controlled by the application of bias current to the tracking range control, pin 7. This pin has no connection as there is no need to reduce the tracking range of the PLL.
8	This is the ground connection of this IC and is connected to ground in the receiver.
9	Pin 9 is a low impedance output terminal for obtaining a demodulated FM signal. If used it must be grounded through a 15000 ohm resistor. There is no way of transmitting a true FM digital signal with this system yet, and this pin is left open.

10 This is a de-emphasis terminal used to demodulate FM audio signals. The information sent on the DSSS system in Stephens' work was audio FM. It is possible to demodulate the signal used in Stephens' work by connecting a 0.01 µF capacitor between this pin and ground, and taking the demodulated output from pin 9.

11 The output of the DBM, J8, is the RF/FM signal applied to pin 11. This is the signal the PLL is trying to track.

12 The output of the VCO, pin 3, is fed to the second input of the phase comparator, pin 12. There the phases of the input signal and VCO signal are compared and the error signal generated.

13 Low pass filters are connected between pins 13, 14, and ground. Each pin has a 0.001 µF capacitor and a variable resistor set for 6000 ohms connected between the pin and ground. These resistors can then be varied as needed to obtain the best loop response time, capture range, and gain. A diagram of this is shown in Figure 10.

14 This pin has the same capacitor and resistor connected to it as pin 13, for the same reasons.

15 See pin 1 connection.

16 This is the power supply connection for the IC. Connecting the 13.6 volt power supply of the receiver to this IC would give a current draw of approximately 10 ma, 13.6 volts / 1500 ohms. This is within the capability of the supply and operating range of the IC.

In order to obtain the 424.6 MHz needed to mix the incoming signal down to 21.4 MHz, it is necessary to install another oscillator. There is no easy way to develop 424.6 MHz from the frequencies present in the AFIT system. By using a 17 MHz oscillator IC chip and passing the output through a pair of X5 frequency multipliers, a frequency of 425 MHz is obtained. This is close enough to 424.6 MHz for the circuit to operate, as the only frequency critical components will be the bandpass filter. A possible bandpass filter can be obtained from the Electronic Engineers Master Catalog. A suitable choice is the Mini-Circuit model PIF 21.4 on page 1822 of Vol A. This filter is centered at 21.4 MHz with a bandpass range of 18 MHz to 25 MHz. Another DBM is needed to combine the 446 MHz and 425 MHz signals to obtain the IF signal of approximately 21 MHz.

Summary

In this chapter were formulas on free running frequency calculations and loop low pass filter equations. The value of capacitance needed to set the free running frequency for each PLL chip was derived. The connections for installation of a PLL in the AFIT DSSS system are also included in this chapter. The NE562B is the PLL IC of choice for installation in this system.

VII. Conclusions.

This chapter contains recommendations and conclusions based on the previous chapters' evaluations and comparisons. The objective of this research effort was to analyze and predict the performance of several different synchronization methods for the AFIT Direct-Sequence Spread Spectrum system. The modular construction of the AFIT system eases the implementation and evaluation of any subsystem component design change. This objective was met and several recommendations were made concerning synchronization methods.

Recommendations

Based on the theoretical performance of the synchronization methods evaluated in this thesis, the convolver matched filter provides the best compromise of advantages and disadvantages. A recommendation is made to implement the convolver matched filter in a future thesis and analyze its performance against the synchronous oscillator presently in use. Theoretically, the matched filter convolver can achieve synchronization in less than

half the time of the synchronous oscillator. This needs to be either verified or disproved. The NE562B phase-locked loop described earlier should be implemented in this system and its operation compared to the synchronous oscillator Stephens constructed.

Some Final Notes

A PLL of this or some other design should be installed in place of the synchronous oscillator in the receiver and its performance evaluated. Uzunoglu claims the SO is much faster at synchronizing with a greater tracking range, but the theoretical values for synchronization times show the PLL is faster. The type of system used makes a difference in the synchronization time.

Another research area of interest is to implement a synchronization method, such as the matched filter convolver, for initial acquisition of the signal and then use a phase-locked loop for tracking the signal after synchronization is accomplished. Tracking range, signal-to-noise ratio of the locked signal, and tracking response time are just a few of the parameters that could be examined.

Bibliography

1. Dixon, Robert C. Spread Spectrum Systems, (Second Edition). New York: John Wiley & Sons, 1984.

2. Dixon, Robert C. "Why Spread Spectrum ?," Class handout distributed in Course 699, Synchronization in Spread Spectrum Systems. School of Engineering and Applied Science, The George Washington University, Washington D.C., May 1985.

3. Eichinger, B.O. and M. Kowatsch. "Combined Matched-Filter/Serial-Search Acquisition Concept for Direct-Sequence Systems," IEEE MILCOM: Military Communications Conference. Vol 1, 305-310 (1987).

4. Gardner, Floyd M., "Comments on Synchronized Oscillators," Proceedings of the IEEE. Vol. 75, No. 8, (August 1987).

5. Gardner, Floyd M., "Phaselock Techniques," (Second Edition). New York: John Wiley & Sons, 1979.

6. Heath Company. "Phase-Locked Loops," (First Edition). Continuing Education Home Study Course. Heath Company, Benton Harbor, Michigan, 1979.

7. Kesteloot, Andre'. "A Practical Direct-Sequence Spread Spectrum UHF Link," QST Magazine, 5:14-21 (May 1989).

8. Kosbar, K.L. "Optimized Cross Correlation Waveforms for First Order Correlation Loops," IEEE MILCOM: Military Communications Conference. Vol 1, 156-160 (1990).

9. Luecke, James R. "Comparison of Detection Schemes for Fast Acquisition Direct-Sequence Spread-Spectrum Receivers," IEEE MILCOM: Military Communications Conference. 865-869 (1989).

10. Ormondroyd R.F. and K.V. Ravi. "Performance of the Serial-Search PN Code Acquisition Techniques Using Monte Carlo Simulation- A Comparative Evaluation," IEEE MILCOM: Military Communications Conference. Vol 2, 791-797 (1991).

11. Pezzolo, Donald E. "Low Cost Spread Spectrum Systems," IEEE ICCE: International Conference on Consumer Electronics. 96-98 (1989).

12. Rappaport, Stephen S. and Donald M. Grieco. "Spread Spectrum Signal Acquisition: Methods and Technology," IEEE Communications Magazine. 22: 6, 6-21 (June 1984).

13 Sklar, Bernard. Digital Communications - Fundamentals and Applications. Englewood Cliffs, N.J.: Prentice Hall, 1988.

14. Stephens, James P. Direct-Sequence Spread Spectrum System. MS Thesis AFIT/GE/ENG/90J-02. School of Engineering, Air Force Institute of Technology (AU), Wright-Patterson AFB, OH, June 1990.

15. Todorvic, Branislav M. "The Impact Of Imperfect Code Synchronization on Bit Error Rate in DS-SS Systems: Upper and Lower Bound," IEEE MELCON: Mediterranean Electrotechnical Conference. 524-527 (1989).

16. Uzunoglu, Vasil and Marvin H. White. "Some Important Properties Of Synchronous Oscillators," Proceedings of the IEEE. Vol. 74, No. 3, (March 1986).

17. Uzunoglu, Vasil and Marvin H. White. "The Synchronous Oscillator: A Synchronization and Tracking Network," IEEE Journal of Solid State Circuits. Vol. SC-20, No. 6, (December 1985).

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The purpose of this study is to analyze and evaluate the performance of several code synchronization methods that could be used in the Air Force Institute of Technology's (AFIT) Direct-Sequence Spread Spectrum (DSSS) communication system. These methods include the sliding correlator, transmitted reference, sequential estimation, and three types of matched filters. The matched filters are the baseband matched filter, delay line matched filter, and the convolver.

The criteria used for the evaluation of these synchronization methods are theoretical synchronization times and probability of bit-error. Advantages and disadvantages of each synchronization method are described and a method is recommended to be tested in the existing AFIT DSSS system prototype.

The effect of adding a PLL circuit to the AFIT system needs to be investigated, especially the effect on the bit-error curve measured by James Stephens when he built the AFIT system. A matched filter convolver should be added in place of the synchronous oscillator.

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